Code.No: **A109210203** | **R09** | **SET-1**

II B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, ECC, ETM, ICE)

Time: 3hours **Max.Marks:75**

Answer any FIVE questions
All questions carry equal marks

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1.a) Derive an expression for total diode current starting from Boltzmann relationship in terms of the applied voltage.

b) The reverse saturation current of a silicon p – n function diode at an operating temperature of 27^0C is 50 nA. Compute the dynamic forward and reverse resistances of the diode for applied voltages of 0.8 V and -0.4 V respectively. [15]

2.a) Define the following terms of a rectifier and filter:
i) Ripple Factor ii) Regulation
iii) Rectification Efficiency iv) Form Factor

b) What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220μF capacitor before delivering to a resistive load of 120Ω? Compute the value of the capacitor for the ripple factor to be less than 15%. [15]

3.a) With the help of input & output characteristics, explain the operation of a BJT in Common Emitter Configuration.

b) For an NPN transistor with α_N = 0.98, J_{CO} = 2μA and I_{EO} = 1.6μA connected in Common Emitter Configuration, calculate the minimum base current for which the transistor enters into saturation region. V_{CC} and load resistance are given as 12 V and 4.0 KΩ respectively. [15]

4.a) Explain how self biasing can be done in a BJT with relevant sketches and waveforms.

b) Design a self bias circuit for the following specifications:
V_{CC} = 12 V; V_{CE} = 2V; I_C = 4mA; h_{fe} = 80. Assume any other design parameters required. Draw the designed circuit. [15]

5.a) Explain the concept of biasing for amplification and principle of amplification with a BJT.

b) For a transistor amplifier, show that the input resistance R_i is given by $R_i = \frac{h_i}{(1 - hrAv)}$. [15]

6.a) Detail the construction of an n-channel MOSFET of depletion type. Draw and explain its characteristics.

b) A self biased p – channel JFET has a pinch – off voltage of V_P = 5 V and I_{DSS} = 12 mA. The supply voltage is 12 V. Determine the values of R_D and R_S so that I_D = 5 mA and V_{DS} = 6V. [15]

7.a) Draw the symbol and equivalent circuit of a UJT. Explain the operation of UJT with the help of its V – I characteristics.

b) With the help of relevant schematic, explain the functioning of a common amplifier. [15]

8.a) Explain how a variable capacitance can be built using a varactor diode.

b) Compute the zener and load currents, power dissipation in the zener diode for the voltage regulator drawn below. [15]

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Time: 3hours **Max.Marks:75**

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1.a) Explain the operation of silicon p – n junction diode and obtain the forward bias and reverse bias Volt – Ampere characteristics.

b) Obtain the transition capacitance C_T of a junction diode at a reverse bias voltage of 12 V if C_T of the diode is given as 15 PF at a reverse bias of 8 V. Differentiate between transition and diffusion capacitances. [15]

2.a) Derive expressions for ripple factor of a Full Wave Rectifier with and without a capacitive filter.

b) Compute the average and RMS load currents, TUF of an unfiltered centre tapped Full Wave Rectifier specified below.
Input voltage to transformer = 220 V/50 Hz.
Step down ratio of centre tapped transformer = 4:1(Primary to each section secondary).
Sum of transformer secondary winding in each secondary segment and diode forward resistance = 100Ω.
Load resistance, R_L = 220Ω. [15]

3.a) Compare the characteristics of a BJT in CB, CE and CC configurations.

b) A Silicon BJT is connected in common Emitter configuration with collector – to – Base bias. Calculate the base resistance R_b for the quiescent collector – to – Emitter voltage, V_{CE} has to be 4 V. V_{CC} and R_C are given as 12 V and 1 KΩ respectively. Assume β = 100, V_{BE} to be zero volts. Also find the stability factor of the circuit. [15]

4.a) Explain how biasing is provided to a transistor through potential divider bias. List the assumptions made. List the need of bias compensation methods.

b) An NPN transistor with β = 50 is used in common Emitter configuration with V_{CC} = 10V and R_C = 2.2 KΩ. Biasing is done through a 100 KΩ resistance from collector – to – Base. Assuming V_{BE} to be zero volts, Find
i) The quiescent point
ii) The stability Factor, 'S'. [15]

5.a) Draw the hybrid equivalent circuit of an NPN – BJT in CE configuration. Derive the expressions for A_V, A_I, R_{in} and R_O.

b) Determine Zi, Zo and AV for the following network for the specifications listed below.
H_{fe} = 110; h_{ie} = 1.1 kΩ; $h_{re} = 2\times10^{-4}$ and hoe = 20 μA/V [15]

6.a) Explain the significance of threshold voltage of a MOSFET. Discuss the methods to reduce threshold voltage, V_T.

b) A FET follows the relation $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$. What are the values of I_D and g_m for V_{GS} = -1.5 V if I_{DSS} and V_P are given as 8.4 mA and -3V respectively. [15]

7.a) With a neat schematic, explain how amplification takes place in a common drain amplifier.

b) Describe the application of a UJT as a relaxation oscillator. [15]

8. Explain the principle of operation of the following devices:

a) Schottky Barrier diode

b) Tunnel diode through Energy band diagrams. [15]

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Time: 3hours **Max.Marks:75**

Answer any FIVE questions
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1. Difference between
   i) Static and dynamic resistances of a p – n diode.
   ii) Transition and Diffusion capacitances of a p – n diode.
   iii) Volt – Ampere characteristics of a single silicon p – n diode and two indetical silicon p- n diodes connected in parallel.
   iv) Avalanch and zener break down mechanisms. [15]

2.a) Define Ripple factor and form factor. Establish a relation between them.
   b) Explain the necessity of a bleeder resistor in an L – section filter used with a Full Wave filter.
   c) Compute ripple factor of an L – section choke input filter used at the output of a Full wave rectifier.nd capacitor values of the filter are given as 10 H and 8.2 µF respectively. [15]

3.a) Describe the significance of the terms, ‘α’ and ‘β’. Establish a relation between them.
   b) A transistor is operated at a forward emitter current of 2 mA and with the collector open – circuited. Assuming $\alpha_N = 0.98$, $I_{EO} = 1.6$ µA and $I_{CO} = 2$ µA, determine
   i) The junction voltages V_C and V_E
   ii) The collector to Emitter voltage V_{CE}
   iii) The region of transistor operation (Saturation/Active/Cut-off).
   Assume any other values necessary. [15]

4.a) Justify statement “Potential divider bias is the most commonly used biasing method” for BJT circuits. Explain how bias compensation can be done in such biasing through diodes.
   b) An NPN transistor with β = 100 is used in common Emitter configuration with Collector – to – Base bias. If VCC = 10 V, RC = 1 K and VBE = 0 V, determine
   i) R_b such that quiescent Collector – to – Emitter Voltage is 4V.
   ii) The stability factor, ‘S’. [15]

5.a) Define all the four hybrid parameters of a BJT in CE configuration. Draw the circuit and its equivalent circuit.
   b) The source and load resistances connected to a BJT amplifier in CE configuration are 680Ω and 1 KΩ respectively. Calculate the voltage gain A_V and the input resistance R_i if the h-parameters are listed as $h_{ie} = 1.1$ kΩ; $h_{re} = 2\times10^{-4}$; $h_{fe} = 50$ and $h_{oe} = 20$ µmhas. Compute A_V and R_i using both approximate and exact analysis. [15]

6.a) Explain how a FET can be made to act as a switch.
   b) Show that the transconductance, gm and drain current, IDS of a FET are related through $g_m = \frac{2}{|V_P|}\sqrt{I_{DSS}\ I_{DS}}$
   Define other terms of the equation.

c) List any four merits of MOSFET to show that they are more suitable than JFETS in Integrated circuits. [15]

7.a) With the help of a neat schematic, explain the functioning of a common source amplifier.

b) Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers. [15]

8.a) What is schottky effect? Elaborate schottky effect for the functioning of a schottky Barrier diode.

b) Describe the construction, principle of operation and performance characteristics of a Silicon controlled Rectifier. [15]

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Time: 3hours **Max.Marks:75**

Answer any FIVE questions
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1.a) Define the following terms for a PN diode
i) Dynamic resistance ii) Load line
iii) Difference capacitance iv) Reverse saturation current

b) A reverse bias voltage of 90V is applied to a Germanium diode through a resistance R. The reverse saturation current of the diode is 50 μA at an operating temperature of 25^0C. Compute the diode current and voltage for
i) R = 10 MΩ ii) R = 100 KΩ [15]

2.a) List out the merits and demerits of Bridge type Full Wave rectifiers over centre tapped type Full Wave rectifiers.

b) The secondary voltages of a centre tapped transformer are given as 60V-0V-60V the total resistance of secondary coil and forward diode resistance of each section of transformer secondary is 62 Ω. Compute the following for a load resistance of 1 KΩ.
i) Average load current
ii) Percentage load regulation
iii) Rectification efficiency
iv) Ripple factor for 240 V/50Hz supply to primary of transformer.

c) What is bleeder resistance in L – section filters? [15]

3.a) Describe the functioning of a BJT in common base configuration.

b) Determine the collector current of a BJT with both of its junctions reverse biased. Assume I_{CO} = 5μA, I_{EO} = 3.58 μA, αN = 0.98 and any other parameter values as required.

c) How do you identify the region of operation of a BJT to be saturation region from the values of various circuit currents? [15]

4.a) Describe the significance of operating point, DC and AC load lines to ensure active region operation of a BJT in CE amplifier application.

b) Calculate the Q – point for the DC biased circuit shown below. [15]

5.a) With the help of a hybrid equivalent circuit of a BJT amplifier, derive expressions for voltage gain and current gain when the source and load resistances of finite values are connected.

b) List out the typical values of h – parameters in the three BJT configurations (CE, CB and CC).

c) Describe how h_{ie} and h_{fe} can be determine from BJT characteristics. [15]

6.a) Differentiate between enhancement and depletion modes of a MOSFET with the help of its characteristics and construction.

b) Determine the pinch off voltage for an N – channel silicon. JFET if the thickness of its gate region is given as 3.2×10^{-4} cm and the donor density in n-type region is $1.2\times10^5/cm^3$.

c) Establish a relation between the three JFET parameters, μ, r_d and g_m. [15]

7.a) Describe how a FET can be used as a voltage variable Resistance (VVR).
b) With the help of circuit diagram and its equivalent circuit of a source follower, derive an expression for the voltage gain possible. [15]

8. Describe the following briefly:
a) Principle of operation of a photodiode.
b) Energy band structure and V – I characteristics of a tunnel diode. [15]

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